Siemens EDA Forum Seoul 2023 AGENDA

09-00 - 10:00	**등록 및 데모부스 관람**
10:00 - 10:10	**Welcome Speech** **김준환 대표이사,** Siemens EDA
10:10 - 10:55	**Keynote I : 불확실성의 시대를 극복하는 강력한 성장 동력** **Joseph Sawicki**, Executive Vice President, IC EDA, Siemens EDA
10:55 - 11:20	**Keynote II : 고객 인게이지먼트를 위한 첨단 프로세스 및 파운드리 솔루션에서의 설계 과제** **Sangyun Kim CVP,** Foundry Design Technology, Samsung Electronics
11:20 - 11:45	**Keynote III : 데이터센터에서 동영상 워크로드의 가속처리** **Donggyu Kim**, CTO, BLUEDOT
11:45 - 13:00	**점심식사 및 데모부스 관람**

Technical Sessions	Track 1 **IC Front-end**	Track 2 **IC Front-end**	Track 3 **IC Back-end**	Track 4 **IC Back-end**	Track 5 **Board Systems**
13:00 - 13:35	**Automated Fault Campaign Flow For Automotive SOC** **Ann Keffer**, Product Marketing Manager, Functional Safety Verification, Siemens EDA **차대서 수석**, System LSI, 삼성전자	**High-Level Verification - What does Verification Look Like in an HLS/C-level Flow?** **이준석 부장**, Siemens EDA	**Trust but Verify Your IP with Solido Crosscheck** **이성민 과장**, Siemens EDA	**Siemens EDA 3DIC Solution overview** **김경록 부장**, Siemens EDA	**Power module design and verification** **장성혁 상무**, Siemens EDA
13:35 - 14:10	**Improving Test Quality and Reliability for Automotive ICs via In-system/In-field Testing** **최윤지 대리**, Siemens EDA	**Raising the Performance of Intelligent Analytics in Complex Ics** **이수용 전무**, Siemens EDA	**Production-accurate .lib Generation and Validation using Solido Characterization Suite** **곽아영 차장**, Siemens EDA	**Automated physical and logical integrity verification for 3DIC with Calibre 3DSTACK** **채동규 대리**, Siemens EDA **김민경 Staff Engineer**, 삼성전자	**DFM verification using ValorNPI & VPL** **김현재 과장**, Siemens EDA **최우섭 프로**, 한화 NxMD
14:10 - 14:45	**Tessent Streaming Scan Network (SSN): Packetized test delivery for complex SoCs** **이윤동 차장**, Siemens EDA	**Veloce proFPGA prototyping solution enables early FW/SW development** **Martin Langner**, Global Account Technology Manager, Veloce proFPGA, Siemens EDA	**Fast, scalable power integrity solution with Calibre mPower** **강경한 부장**, Siemens EDA	**The Next Frontier in Memory Testing : 3D IC SRAM Test Methodology for High-Quality Products** **이재훈 파운드리 설계기술,** 삼성전자	**Digital Transformation using Xpedition & TeamCenter** **홍중배 상무**, Siemens EDA
14:45 - 15:10	**커피브레이크 및 데모부스 관람**				
15:10 - 15:45	**Power Optimization for Low-power Designs with an Early Power Methodology** **변민섭 이사**, Siemens EDA	**Unlock the Potential of Digital Methodologies with Symphony for Improved AMS Verification Throughput and Debug Productivity** **임택규 이사**, Siemens EDA	**Reinforce your design with Calibre VIA Enhancer** **문성진 과장**, Siemens EDA **권용진 책임연구원**, LG전자	**Intrinsic Intelligence P&R for Advanced Node Designs** **Henry Chang,** Sr. Director, Aprisa Product Management, Siemens EDA	**Advanced Packaging Layout using XPD** **노상목 사원**, Siemens EDA
15:45 - 16:20	**Early power trend analysis with end-user software, power aware verification and power sign-off with Veloce** **이규언 이사**, Siemens EDA	**Lint and Advanced Lint as a Sleep Aid** **방실이 차장**, Siemens EDA	**CalibreKR CheckStore – Voltage Check** **변선수 부장**, Siemens EDA	**Implementing RealTime Digital and signoff metal fill in the P&R design environment for faster and more accurate tapeouts.** **이훈구 부장**, Siemens EDA	**PCB Design Optimization using HyperLynx** **김안국 이사**, Siemens EDA
16:20 - 16:30	**경품추첨 및 맺음말**				

SIEMENS